Design and Verification of Ultra Low Power SoCs with ARM Cores

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CAE Manager, VG
Agenda

• Introduction
• Common Power Management schemes on ARM based SOCs
• Typical errors found in power management
• Bug Avoidance and Verification Strategy
• Conclusion
Introduction
Making the leading solution in Power Management Verification

SYNOPSYS ACQUIRES ARCHPRO DESIGN AUTOMATION

ArchPro’s Power Management Technologies to Enhance Synopsys’ Low Power Design and Verification Solution

MOUNTAIN VIEW, Calif., June 18, 2007 - Synopsys, Inc. (Nasdaq:SNPS), a world leader in semiconductor design software, today announced that it has acquired ArchPro Design Automation. ArchPro’s technologies enable engineers to address power management challenges in multi-voltage designs from architecture to RTL to gates.

"ArchPro’s industry-leading technologies are actively used in verification and sign-off of our most advanced multi-voltage designs," said Hisaharu Miwa, general manager, Design Technology Div, LSI Product Technology Unit at Renesas Technology Corp. "Use of innovative low-power design techniques continues to increase rapidly at Renesas. Integration of Synopsys’ market-leading verification technologies including SystemVerilog testbenches, coverage, and assertions with ArchPro’s advanced power management verification techniques will create a unique value-proposition for addressing the exponentially growing verification challenge.”
Power is a huge challenge for IC design

Both dynamic and leakage power are problematic
Dynamic Power Dissipation

\[ P_{\text{dynamic}} = P_{\text{switching}} + P_{\text{shortcircuit}} = \left(0.5 \times C \times V^2 \times \alpha \times f\right) + \left(I_{sc} \times V\right) \]

To reduce dynamic power dissipation

- Reduce voltage
- Reduce capacitance
- Reduce switching activity

Voltage control is key
Static Power Dissipation

\[
P_{\text{leakage}} = \left( I_{\text{sub-threshold-leakage}} \times V \right) + \left( I_{\text{gate-oxide-leakage}} \times V \right)
\]

\[
= \left( K_1 W e^{-V_{th}/nV_e} \left( 1 - e^{-V/V_e} \right) \times V \right) + \left( K_2 W \left( V / T_{ox} \right)^2 e^{-\alpha T_{ox}/V} \times V \right)
\]

To reduce static power dissipation

- Reduce voltage
- Increase threshold voltage
- Improve process technology

Voltage control is key
Power Management Techniques

• Dynamic Power
  ▪ Reduce Voltage
  ▪ Reduce Capacitance (Small Transistors, Short Wires)
  ▪ Reduce Switching activity (Clock-Gating, Sleep Mode)

• Static Power
  ▪ Reduce Voltage
  ▪ Increase threshold voltage (Use of High Vt transistors)
  ▪ Specialize manufacturing process technology

Voltage control techniques can result in up to 2X/10X savings in power
Voltage-Control Techniques

Multi-Voltage (MV)

MTCMOS power gating (shut down)

Power gating with State Retention

Dynamic or Adaptive Voltage Frequency Scaling (DVS, DVFS, AVS, AVFS)

Variable $V_{TH}$ (Back Bias – P/N)

Low-VDD Standby
Voltage Control Has Become The #1 Choice for Power Reduction

BackBias 5%
Retention 15%
DVFS 15%
Voltage scaling 35%
Power gating 30%
Common Power Management Architectures
A typical mobile SOC ...

• Consists of
  ▪ One or more ARM cores
  ▪ Blocks(Islands) that can be independently controlled
    • Plus, Voltage Regulators/Power Switches etc.
  ▪ A hardware power management unit
  ▪ A software driver for power management functions
  ▪ Both Hardware and Software Inputs to the PMU
A typical mobile SOC

PMK controls: Power switches Isolation cells Save/restores

VR

ARM CPU

PMU

Software

Baseband

Gfx/Video

MP3

Could Be Similar Subsystems

Button Press

Battery/Always On

POR Logic

Pin Straps

OTP

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e.g. Smart Phone Wakeup

- Button Press – H/W initiated
  - Activates various parts – keyboard, screen, password routine etc.
- Alarm Clock – S/W initiated
  - Software initiated wakeup on some programmable interrupt function

In reality, h/w and s/w interplay with each other

There could be multiple events in parallel
An Example SmartPhone

ARM IEM – A ready to use h/w-s/w solution- silicon proven

SOC Components

ARM CPU

IEC/APC

PMK controls:
Power switches
Isolation cells
Save/restores

IEM Software

System/Software

IC/SOC

Voltage Regulators

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ARM-Synopsys* Collaborate to Verify IEM+926 based SOC, 06/2005

- 65nm CPU, 3 voltage domains, ARM926 based SOC
  - AVFS, Back Bias, Standby, Power Gating, Retention techniques applied
  - IEM Hardware/Software controller
- 60% dynamic power savings, 8x-10x leakage reduction demonstrated

Completely verified at the RTL and Netlist stages: resulting in first pass silicon success

* ArchPro products were used at that time
Typical Error Situations
Failure to Wakeup

- Run
- Hibernate
- Core
- Power Down
Premature Write ➔ Can’t wake up from Hibernate

CLK Gating Signal released prematurely
Insufficient voltage for write
Unknown value in REG leading to memory corruption

Traditional simulators will not detect this issue because they can’t simulate a voltage ramp
Unsafe Writes ➔ Memory Corruption

- VDD 1.0 V
- CLK
- Q
- MEMORY CORRUPTION BECAUSE OF UNSAFE WRITE

VDD 1.0 V
CLK
Q
0.7 V
0.5 V
D = 0
D = 1

Flip Flop

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Using Off islands to Wakeup!

Inside the chip:

DIGITAL

2.1V

Level Shifter

RSTTEST_out

RST Logic

3.6V

Regulator

2.1V

Regulator

2.5V

V21

V21_ctrl

V25_o

V25_ctrl

RSTTEST

V21_o

Using Off islands to Wakeup!
Conflicting events!

- **Software**: Save context, notify devices and Shutdown → Run the CPU
- **Thermal Overheat**: Gate Clocks, Lower Voltages → Don’t run CPU

Diagram:
- ARM CPU
- VR
- PMU
- POR Logic
Voltage Scheduling Error

Power State Table

<table>
<thead>
<tr>
<th>V1</th>
<th>V2</th>
<th>Need LS?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2V</td>
<td>1.1V</td>
<td>No</td>
</tr>
<tr>
<td>0.9V</td>
<td>0.8V</td>
<td>No</td>
</tr>
</tbody>
</table>

Static Analysis – No level shifter needed

Dynamic Situation – Need level shifter or change Voltage Scheduling
Bad xtiions and Intermediate states

Real xtiion

Intended Xtion – Bad!

Power State Table

<table>
<thead>
<tr>
<th>Power State</th>
<th>V1</th>
<th>V2</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>1.2V</td>
<td>1.2V</td>
</tr>
<tr>
<td>P2</td>
<td>1.3V</td>
<td>1.?? V</td>
</tr>
<tr>
<td>P3</td>
<td>1.3V</td>
<td>1.5V</td>
</tr>
</tbody>
</table>

V1 -> V2 | V2 -> V1
A | No Level Shifter Needed
B | H2L | L2H
C | L2H | H2L
Unplanned State causes Power Gating Collapse

OFF VOLTAGE ISLAND makes unwanted excursion to ON state.
Premature Restore: Don’t race against Voltage

Sensing Voltage Readiness is really tricky!
Combining Multiple CPUs

- Must take a hierarchical sub-system view
- Must be conscious of s/w threads and h/w events in each sub-system
- An “FSM” view of power states must be commonly known across the sub-system boundary
  - E.g ACPI
- Best to enforce a consistent protocol across all sub-systems
  - Industry standards are only emerging here
- Homogeneous subsystems make code-reuse possible
  - A draw back of heterogeneous subsystems, but this is common
Bug Avoidance and Verification Strategy
2 dimensions of Power Management Verification

Voltage Aware Boolean Analysis (Electrical Accuracy)

Hybrid (Static-Dynamic) approach to conquer complexity
Traditional Logic Verification

- Single VDD design
- Bring up period
- Non Logic sim
- “Always On” Logic sim

Vdd → IC
Power Management Verification

- Sequenced Bring up
- Essential to verify

- “Variable Voltage” Logic sim
- Micro-second timescale
- State Triggers
- Asynchronous Handshakes
- Mixed-signal components
- H/w-s/w partitions
- Pre-work, Post-work

System/Software

IC/SOC

Voltage Regulators
Fundamental Technology Shift Enables Verification of Power Management

Traditional Boolean Analysis

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>O</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Voltage-aware Boolean Analysis

<table>
<thead>
<tr>
<th>V1</th>
<th>V2</th>
<th>V3</th>
<th>A</th>
<th>B</th>
<th>O</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
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<td>...</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Don’t confuse this for X-injection!
Why is X-Injection Not Enough?

- Treats voltage as a binary value
  - No Voltage input into boolean equations
- X-Injection can’t detect
  - Logic Conversion Errors
  - Power-on Reset Bugs
  - Voltage Scheduling Errors
  - Unplanned States, Unsafe States
  - Memory Corruption Issues
  - Power Gating Collapse
  - Multi-Fanout Issues
  - Voltage Sensing Handshake issues
  - Aborted Transitions

We need all this and a sophisticated verification methodology
Power Management Increases Verification Complexity

**Design**

- Island 3: Always ON
- Island 1: On/off
- Island 2: On/off
- PMU
- S1
- Top

**Verification**

- Stby1: Off, On
- Low Pwr: Off, Off
- AllOn
- AllOff
- Stby2: On, Off

- Allowed transitions
- Disallowed transitions

• Verification must ensure correctness of:
  - Voltage Isolation Cells

• Verification must be aware of:
  - Power States
  - Voltage Transitions
  - Valid Power Sequences
Traditional Coverage vs. MV Coverage

• Traditional: Directed and Random tests
  ▪ Line, Toggle, FSM, Assertion Coverage
• Multi-Voltage
  ▪ Static Coverage
    ▪ Check isolation cells, level shifters etc.
  ▪ Focused Dynamic coverage in each Power State
    ▪ E.g. No need to cover isolated signals in On block
      ▪ But need to prohibit toggles on off block inputs
  ▪ Dynamic Coverage of Power State Transitions
    ▪ A transition may be caused by more than one activation path
      ▪ E.g. Laptop hibernates because
        Low Battery, Lid close, Inactivity
    ▪ New Assertions to include Voltages, PMU components
      ▪ What are these and how do you write them?
• Can we shift more items from Dynamic to Static?
  ▪ Arch/uArch Analysis, Power Sequence analysis yield a lot of bugs!
Structural Checks - Static

- Island-1: ON(1.2V)/OFF
- Island-2: 0.9 - 1.2V
- Island-3: ON (1.2V)

Protection Cells:
- Missing
- Redundant
- Incorrect type
- Incorrect island
- Isolation polarity
- Incorrect ISO-Enable
- Validates ISO-Enable network
- ISO-Enable polarity

- Level Shifters
- ISO-Enable
- Isolation
Temporal checks – Dynamic and Static

- **SCAN**
- **OFF**
- **CORE**
- **USB**
- **BT**

Power States covered by MVSIM:
- GPS + CODER
- GPS + CODER + MEM
- GPS + MEM
- BT + CODER
- BT + CODER + MEM
- BT + MEM
- USB + CODER
- USB + CODER + MEM
- USB + MEM

Identical Voltage Power States:
- GPS
- GPS + CODER
- GPS + CODER + MEM
- GPS + MEM
- BT + CODER
- BT + CODER + MEM
- BT + MEM
- USB + CODER
- USB + CODER + MEM
- USB + MEM

Only States verified by Traditional Simulators:
- USB
- BT

Power Transitions covered by MVRC:
- GPS → BT
- GPS → USB
- BT → USB
- BT → GPS
- USB → BT
- USB → GPS

- GPS + CODER
- GPS + CODER + MEM
- GPS + MEM
- BT + CODER
- BT + CODER + MEM
- BT + MEM
- USB + CODER
- USB + CODER + MEM
- USB + MEM
Power-Aware Verification Flow

Choose appropriate voltage domains, design styles etc.

System and Software Architecture

RTL Implementation

RTL Verification

Gate Level Implementation

Gate Level Verification

Physical Implementation

Signoff

Manufacturing

MVRC: Arch/uArch Analysis
Overhead est.
Pwr Seq Prediction

MVSIM: Dynamic Coverage
F/W Verification

MVRC: Structural checks
Clk/Reset/Scan rules
Island ordering checks

MVSIM/MVRC: Structural checks
Island ordering checks
PG Checks
POR Sim.

Signoff Tools Must be Voltage-Aware for 1st Pass Silicon Success

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First-Pass Silicon Success With Synopsys (ArchPro)

ArchPro’s comprehensive power management EDA suite offers an effective method to reduce costs and time associated with the design cycles of low-power IC verification and implementation. The tool provides an elegant solution to power management.”

Michael Hurlston
VP and GM, WLAN BU

“EDA tools for dynamic voltage scaling have only recently emerged. ArchPro enables customers to verify their multi-voltage designs early, in the RTL design cycle, thus reducing the risk of non-functional silicon.”

Kevin McIntyre
IEM Product Manager

"ArchPro solutions not only verified our power scheme at RTL level, but also helped us debug some complex problems after the netlist was generated. They really helped us get to the sign-off. We are pleased with their performance and the seamless integration with our flow.”

Yoshio Inoue
Chief Engineer, DFM & Digital EDA

“… to maximize functionality while minimizing power usage. Working with ArchPro is definitely giving us an edge in designing the next generation of complex, multi-voltage SoCs, something we haven’t seen anywhere else in EDA.”

Mohammad Moradi
Founder, CTO

30+ design tape outs over last two years
Next Generation Verification System for Power Management

- Automatic creation of verification plan
  - Profiling of design and power intent and automatic assertion + coverage point creation
- Extended MV-Logical Analysis
  - All combinations of voltage and functional states supported
- Recommended Wake-up and Sleep sequences
  - Based on design and power intent

GUI

- Power Intent Visualization Module
- Static Analysis Engine
- Dynamic Verification

Testbench Power Intent RTL Voltage Aware Models

Assertion Failures Vector Grading

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Conclusion

• A 2X reduction in Dynamic Power and 10x reduction in leakage can be achieved

• Power Management always involves both hardware and software working together – esp. in mobile systems with ARM CPUs

• Verification of Power Management schemes is tricky and escapes traditional boolean analysis

• An effective verification strategy utilizes both static and dynamic techniques working together
Thank you!

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