Achieving HD Video Decoding with ARM Processors

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Imagination Technologies
Introduction

- Imagination Technologies
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  - Technology Overview
  - Global Video Market Trends
  - PowerVR Video Core Architecture Roadmap

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  - Hardware Architecture
  - Video Standards Supported
  - Performance

- POWERVR VXD370 Software Architecture
  - Software Architecture
  - Software Driver APIs

- Typical Application Examples

- Summary
Our Mission:

Deliver flexible, high performance Intellectual Property (IP) that is cost-effective for high volume System On Chip (SOC) applications, and provides inspiration for industry leading product innovation.

- Founded: 1985
- Listed: 1994 - LSE: IMG
- Revenue (2006): £48.1M
- More than 400 employees world-wide, …of which > 80% are engineers
- HQ: UK
- Sales: Japan, US, Taiwan, Korea, China
- R & D: UK, India
Imagination Technologies’ IP cores work together to create industry leading mature solutions for all parts of receiver, processing and display sub-systems of SoCs.
Global Video Market Trends

- Content raising user expectations
  - Driving receiver requirements - “Play anywhere”

- Fixed TV Trends
  - Analogue to Digital transition
  - Internet TV (IPTV)
  - Flat Panel Displays (LCD, Plasma, LCOS…)
  - SD to HD migration
  - Competing Video Codec Standards
  - Encode / transcode functionality to support PVR
  - New Use Cases – Place / Time Shifting, PVR to Mobile

- Mobile Phone / PMP / Mobile TV Trends
  - Increasing screen resolution requirements from QVGA to VGA, WVGA
  - Mobile devices support HD – content playback is important
  - Mobile TV being promoted as next handset ‘killer app’
  - Multiple Video Codec Standards
  - Low power consumption is essential
  - Mobile Media storage by advanced micro HDD’s
POWERVR Video Systems Experience

- Scalable Technology
  - Accelerators to full codec solutions
  - Sub QCIF to multi stream High Definition
  - Multi standard video experience
    - JPEG, MPEG-1, MPEG-2, H.263, MPEG-4, DivX, H.264, VC-1, AVS

- Tested and Proven
  - ~ 3000 Test Streams
  - Internal Imagination, Allegro, Standards Organisations, Customer Supplied
  - 15+ Years Development Experience in Graphics and Video

- Broad Systems Experience
  - Imagination has architected several SoC’s for customers:
    - DTV, STB, Freeview, DAB
    - Full Software inc HDD, DVD, STB higher level components
  - Experience of systems design fed into IP core development
    - Memory bandwidth, memory latency, interrupt latency, …
POWERVR Video Core Architecture Roadmap

**HD Applications**
- STB
- IPTV
- HD-DVD
- BluRay
- DTV
- PVR
- Camcorder

**SD Applications**
- DVD
- PVR
- Mobile Phone
- PMP
- DSC
- Navigation

**Available**

**In Design**

**In Planning**

**Released**
- M2VX Multi Stream MPEG-2 ‘ES Level’

**New**
- VXD370 Multi Stream Multi Standard ‘ES Level’

**Future**
- VXD3xx

**HD Decode**
- MVDA2 Multi Standard Accelerator

**HD Encode**
- VXE250 Multi Standard ‘ES Level’

**SD Decode**
- MVED1 Multi Standard ‘Codec’

**SD Encode**
- VXE2xx

**VXExxx**

**VXD3xx**

**In Planning**

**In Design**

**Released**

**Available**
POWERVR VXD370
High Definition Video Decoder
POWERVR Approach for HD Decoding

- Software-only approach needs more CPU resource than available
  - Especially true for HD resolutions, profiles, and bit rates

- Accelerator approach is also sub-optimal for HD
  - Still requires significant proportion of CPU
    - Limiting processing cycles available to underpin rest of user experience
  - Increases memory bus bandwidth (CPU instruction fetches, data moves)
  - Greater power consumption

- POWERVR approach: Full “elementary stream” HD decoder
  - Minimises memory bus bandwidth and power
  - Affordable area cost, especially with decreasing process geometries
  - CPU reduced to supervisory role
POWERVR VXD370 HD Decoder

- **Standards Supported**
  - VC-1 (WMV 9), H.264, DivX, MPEG-4, H.263, MPEG-2, MPEG-1, JPEG

- **Feature Set**
  - Patented CABAD decoding
  - CAVLD, VLD and Exp-Golomb decoding
  - Inverse scan; Inverse DCT; Integer inverse transform
  - $\frac{1}{2}$, $\frac{1}{4}$ and $\frac{1}{8}$th -pel motion compensation
  - Full support for unrestricted motion vectors
  - Full bi-directional prediction
  - Inverse H.264 intra prediction
  - H.264 de-blocking and VC-1 (WMV 9) de-blocking / overlap filters
  - Support for trick modes and error concealment / recovery
  - MTX Stream Manager for programmable stream header processing
  - Configurable for single, dual, triple or quad stream decode
## POWERVR VX D370 Supported Profiles

<table>
<thead>
<tr>
<th>Standard</th>
<th>Profile @ Level</th>
<th>Maximum Bit Rate (~ bps)</th>
<th>Resolution</th>
<th>Frame Rate (fps)</th>
<th>Format</th>
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<tr>
<td>H.264</td>
<td>BP@L3</td>
<td>10M</td>
<td>720 x 576, 720 x 480</td>
<td>25, 30</td>
<td>PAL</td>
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<td>NTSC</td>
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<td>H.264</td>
<td>MP@L4.1</td>
<td>50M</td>
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<td>30, 30, 60</td>
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<td></td>
<td>720p</td>
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<td>384K</td>
<td>352 x 288, 320 x 240</td>
<td>15, 24</td>
<td>CIF</td>
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<td>VC-1 (WMV 9)</td>
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<td>20M</td>
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<td>25 / 30</td>
<td>1080p</td>
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<td>AP@L3</td>
<td>45M</td>
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<td>720p</td>
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Note: * ASP using SP toolset
POWERVR VXD370 Performance Benefits

- **Low Silicon Area**
  - 65nm: 2.9mm²
  - 90nm: 4.9mm²
  - 130nm: 9.8mm²

- **Low Clock Speed**
  - Single HD 1080i HP@L4.1 H.264 decode: 133 MHz
  - Dual HD decode 1080i HP@L4.1 H.264 decode: 266 MHz
  - Simultaneous single HD & single SD decode: 180 MHz

- **Low Power – 90nm LP**
  - Single 1080i H.264 HP@L4.1 decode: 45mW
  - Single 1080i MPEG-2 MP@HL decode: 32mW

- **Most technically competitive multi-standard HD decoder IP available today**
POWERVR VXD370
Video Software Architecture
POWERVR VXD370 Software

- Win32 Visual Development and Test Framework
  - FPGA based test system – being demonstrated on our stand
  - Bulk testing of video streams

- MS DXVA 2.0 Drivers for MS Vista
  - Supports VLD and MC entry points
  - Slice level switching

- Embedded System Drivers/APIs
  - STB, PVR, DVD, HD-DVD, Blu-Ray, DTV etc.
  - Provides full ES level (or equivalent) parsing/decoding

- VXD370 MTX Stream Manager Firmware
  - Binary code for MTX Stream Manager within the video decoder IP Core
  - Base layer section + section for each video standard
  - Decodes bit stream headers from ES Level, NAL units etc.
POWERVR VXD370 Software Architecture

- ARM CPU
- Video Application
- Host OS
  - POWERVR VIDDEC API
  - POWERVR DMAC API
- SDRAM Frame Buffers
- FLASH OS Firmware POWERVR Drivers

POWERVR VXD370
- Firmware Base Layer
- MTX Stream Manager
- Base Hardware

Supported Formats:
- H264
- VC-1
- MPEG4
- MPEG2
Embedded Systems Software

1) Host CPU Reference Software (ANSI C Source)
   - An example of how to “use” the embedded APIs
   - Responsible for sourcing the ‘ES Level’ bit stream
   - Performs buffer & frame management

2) Embedded APIs (ANSI C Source)
   - Designed for embedded real time systems
   - Built on abstraction layer to simplify OS porting
     - Basic OS features only - tasks, interrupts and semaphores

3) MTX Stream Manager Firmware (Binary)
   - Performs bit stream header parsing
   - Control of multi-mode hardware blocks which decode at macroblock and block levels
   - Simple messaging interface between Host CPU Software and MTX Stream Manager Firmware
VIDDEC Driver API Components

- VIDDEC Driver/API core
  - Functions called by video application

- LISR (Low Level Interrupt Service Routine)
  - Invoked when a device interrupt occurs

- HISR (High Level Interrupt Service Routine)
  - Normally runs in the context of a high-priority task
  - Provides the context in which the application event callback function is called
  - Callback can make blocking calls into the OS or calls back into the driver/API
Porting Drivers / APIs

- Video Application
- VIDDEC Driver / API Core
- Application Callback
- HISR
- LISR
- ISR API
- Target Abstraction Layer (TAL)
- OS Adaptation Layer (OSAL)
- Underlying OS

Abstraction APIs

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ARM Developers’ Conference & Design Pavilion 2007
Porting Drivers / APIs

- OS Adaptation Layer (OSAL)
  - Adapts the API to the underlying operating system

- Interrupt Service Routine API (ISR)
  - Abstracts the interrupt handling and the binding between the LISR and HISR

- Target Abstraction Layer (TAL)
  - Abstracts the hardware access from the Driver or API

- VXD370 Driver Porting involves:
  - the creation of a OSAL and TAL
  - Adaptation of the ISR module for the platform
POWERVR VIDDEC API

- Simple API usage model
- Essentially to decode video the process is:

  Initialise (the API)
  Configure (the core)
  Locate decode entry point (find start of stream)
  Get stream information (discover video stream)
  Locate picture decode point (find start of picture)
  While (not end of stream) {
    Get picture information (decode video)
    Decode picture
  }

Basic VIDDEC Functions Calls

// Initialise VIDDEC API
VIDDEC_Initialise();

// Initialise VXD370 – multi video core system possible
VIDDEC_DeviceInitialise( ui32DeviceNo );

// Configure the video core
VIDDEC_DeviceConfigure( ui32DeviceNo, sConfigData );

// Initialise a stream on the video core
VIDDEC_StreamInitialise( ui32DeviceNo, ui32StreameNo );

// Setup a callback to handle device/stream events
VIDDEC_StreamAddEventCallback( ui32DeviceNo, ui32StreameNo, VIDDEC_EVENT_ALL,
                                &CbFunc, &sCbData, &hEventCallback );

// Configure the stream for a given standard - this is an asynchronous operation
VIDDEC_AsyncStreamConfigure( ui32DeviceNo, ui32StreameNo, sStreamConfigData );

**** Wait for VIDDEC_EVENT_STREAM_CONFIGURE_COMPLETE event
Basic VIDDEC Functions Calls

**** Start asynchronous task to DMA bit stream data (ES level data)

// Locate a decode entry point
VIDDEC_AsyncStreamEnableInput( ui32DeviceNo, ui32StreamNo,
    VIDDEC_INPUTMODE_LOCATE_DECODE_ENTRY_POINT, sInputControl );

**** Wait for VIDDEC_EVENT_LOCATE_DECODE_ENTRY_POINT_COMPLETE event

// Get header information - used to configure buffers etc.
VIDDEC_StreamGetHeaderInfo( ui32DeviceNo, ui32StreamNo, &sHeaderInfo);

// Locate a picture decode point
VIDDEC_AsyncStreamEnableInput( ui32DeviceNo, ui32StreamNo,
    VIDDEC_INPUTMODE_LOCATE_PICTURE_DECODE_POINT, sInputControl );

**** Wait for VIDDEC_EVENT_LOCATE_PICTURE_DECODE_POINT_COMPLETE event
Basic VIDDEC Functions Calls

while (!bEndOfStream) {
    // Get picture type
    // Used to performance reference frame management etc.
    VIDDEC_StreamGetPictureType( ui32DeviceNo, ui32StreameNo, &sPictureTypeInfo );

    // Decode picture
    VIDDEC_AsyncStreamEnableInput( ui32DeviceNo, ui32StreameNo,
                                   VIDDEC_INPUTMODE_DECODE_NEXT_IMAGE, psInputControl );

    **** Wait for VIDDEC_EVENT_PICTURE_DECODE_POINT event or “end of stream”
}

****
ARM CPU based HD Video Decoder
Application Specific Examples
STB Software Components

- Application Software
  - Set up and control
  - Transport Stream Demux
  - Video Decode
  - Display Output

- Display Manager
  - Passes video buffers between output manager and the pixel display pipeline
  - Handling any display control requirements
    - re-sizing, display positioning etc.

- A/V Sync Manager
  - Provides control information for the Display Manager to enable it to present images at the correct time
HDD Playback Software Components

- Hard Disk Playback capability

- Application File Read Callback
  - Responsible for:
    - Call to source bit stream data from the HDD media
    - Accessing bit stream on hard disk

- Application Playback Control
  - Responsible for:
    - Set up and control of the TS Demux, A/V decode, HDD playback and output

- SMHDP API
  - Responsible for:
    - Supports normal playback
    - Trick mode playback i.e. fast / slow, forward / reverse etc.
    - Video and audio decoders are bound together and controlled as a single stream
DVD Playback Software Components

- DVD Playback capability

- Application VOB Read Callback
  - Responsible for:
    - Calls to source bit stream data
    - Accessing DVD VOB data

- Application Playback Control
  - Responsible for the setup and control of:
    - TS Demux, decode, DVD navigation and output

- Display Manager
  - Responsible for
    - Passing video buffers between the output manager and the pixel display pipeline
    - Handling any display control e.g. re-sizing, display positioning etc.
Summary

- POWERVR VDX370 HD Video Decoder:
  - Mature and proven IP core
  - High Performance (low clock, small die area)
  - Widest range of video codec standards
  - Comprehensive Software Support
    - Build your own system – simple porting
    - Use IMG tried and tested software architecture
    - Khronos OpenMAX support on the way
  - Easy to Port to ARM Based CPU’s

- The leading HD Video Decode solution for ARM CPU’s
Thanks and Questions?

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