Design Techniques for 45nm SOI Technology

Christophe Frey
Engineering manager – SOI design center
Agenda

- SOI introduction
- SOI design Challenges
- Standard cell design
- IO design
- History effect characterization
- Memory design
SOI introduction

- **SOI: Silicon On Insulator**
  - Refers to the use of an SOI wafer
  - Variable thickness
    - Top silicon film
      - Thick film $> 300\text{nm}$
      - Thin film $< 300\text{nm}$
    - Buried oxide $< 1\mu\text{m}$
  - Electrical behavior of SOI transistors related to top silicon thickness
    - Thick film: similar to bulk CMOS (body not floating)
    - Thin film: **partially depleted** or fully-depleted (body floating)
Performance benefits of SOI cmos

- **Speed**
  - Reduced junction area & capacitance
  - Threshold voltage (Vt) dyn lowering
    - More current at same Vdd
    - Same speed at lower Vdd, → lower power

- **Area**
  - Denser circuit layout
    - No well ties
    - Reduced transistor spacing
  - Higher SOI transistor drive current
    - Synthesis tool will pick smaller cell in SOI for a given C load
45nm SOI vs 45nm Bulk

Targeting highest speed for bulk & SOI
→ SOI 42% faster w/ 10% lower power

<table>
<thead>
<tr>
<th></th>
<th>SOI</th>
<th>Bulk</th>
<th>%SOI –Bulk/bulk</th>
</tr>
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<tbody>
<tr>
<td>Frequency (GHz)</td>
<td>1.24</td>
<td>0.87</td>
<td>42%</td>
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<tr>
<td>Leakage power (µW)</td>
<td>0.65</td>
<td>0.40</td>
<td>+64%</td>
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<tr>
<td>Dynamic power (µW/MHz)</td>
<td>0.80</td>
<td>0.88</td>
<td>-10%</td>
</tr>
<tr>
<td>Total power @ 500Mhz (µW)</td>
<td>399</td>
<td>441</td>
<td>-10%</td>
</tr>
<tr>
<td>Area</td>
<td>same</td>
<td></td>
<td></td>
</tr>
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</table>

Targeting same speed in bulk & SOI
→ 40% less power & smaller area (smaller drives)

<table>
<thead>
<tr>
<th></th>
<th>SOI</th>
<th>Bulk</th>
<th>%SOI-Bulk/ bulk</th>
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<tr>
<td>Frequency (GHz)</td>
<td>0.93</td>
<td>0.87</td>
<td>7%</td>
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<tr>
<td>Leakage power (µW)</td>
<td>0.33</td>
<td>0.40</td>
<td>-17%</td>
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<tr>
<td>Dynamic power (µW/MHz)</td>
<td>0.54</td>
<td>0.88</td>
<td>-40%</td>
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<tr>
<td>Total power @ 500Mhz (µW)</td>
<td>268</td>
<td>441</td>
<td>-40%</td>
</tr>
<tr>
<td>Area</td>
<td>reduced in SOI</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- SOI demonstrates strong PPA advantage over bulk CMOS for digital designs
  - Brings back flexibility for design optimization
  - Can be achieved using standard EDA flow and physical IP`
SOI design challenges

- Standard cell design
- IO design
- History effect characterization
SOI Design Challenges

- SOI specific design requirements
  - Spice simulation: Dedicated SOI models
    - Most of the industry using BSIMSOI
  - Floating body effect
    - History effect
    - Parasitic bipolar effect
      - Additional characterization & specific modeling techniques
      - Design techniques to suppress or limit history effect
- ARM has expertise & flows to manage those effects
- Direct migration from bulk IP to SOI usually doesn’t provide expected PPA benefits
Parasitic bipolar effect in an SOI transistor

- Body is floating and D/S variations couple to the body
  - Body dynamic behaviour is important

- Body is the base of the parasitic bipolar
  - \( V_{bs} = V_{be} \) determines the amount of bipolar current

- D/S can couple charges to the floating body
  - \( V_t \) of the transistor is changed (good for speed)
  - But D can couple to S through floating body
Standard cells

- Design sensitivity to SOI
  - Some SOI specific effects may impact functionality
  - Sequential cells architecture must be carefully selected to avoid functional failure

- Timing sensitivity to SOI
  - Floating body effects are state and transition dependent
  - Standard cells are used for random logic, thus history effects are unavoidable
  - Careful timing characterization is necessary
Standard cell functional failure example

Latch with passgate is not safe!

\[ I_{\text{bipolar}}: \text{with floating body} \]

\[ V_{BE} = 0.8V \]

\[ 0.15\mu m \text{ technology} \]

ARM Developers’ Conference & Design Pavilion 2007
45nm SOI sequential cell functionality

- Parasitic bipolar is not activated in this technology
- S to D coupling through body start being visible
- But latch with passgate is safe

![Diagram of a 45nm SOI sequential cell]

Vbs = Vbe = 0.32V

ARM Developers’ Conference & Design Pavilion 2007
SOI IO design

- IO cells are quite different
  - no guard rings needed in SOI as there is no latch-up
  - body-tied transistors used to improve breakdown voltage in the high-voltage domain
    - parasitic bipolar reduces breakdown voltage of FB transistors
  - ESD protection devices use thin silicon film
    - no bulk junction (without opening buried oxide)
    - related to total width of the devices
    - off-state wide NMOS for power clamp
    - gated or non-gated diode (lateral junction)
  - Layout and schematics differ
SOI IO design

- ESD protection: RC-triggered power clamp
  - uses body-tied transistor
  - FB transistor may be used in low-voltage domain
  - leakage current reduced

- Voltage tolerant IO \( (i.e \; voltage > \text{maximum tolerated for the transistor (e.g. 3.3V/2.5V)})\)
  - SOI dielectric isolation greatly facilitates the implementation
  - BULK requires isolated well (triple-well process) if drain-body junction breakdown voltage < high voltage (3.6V WC)
  - No body effect \( (vbs=0) \rightarrow \) smaller nmos
History effect timing characterization

- Body potential depends on the history of the devices.
- We commonly define two dc states:
  - DC0: input is low (0V)
  - DC1: input is high (Vdd)
History effect (HE)

- Depends on many parameters
  - Process, voltage, temperature ➔ PVT corner
  - Circuit frequency and activity
  - Input slew
  - Output load
  - Other inputs switching for multi-input cells

\[ T_{pHL1A\_DC00} \neq T_{pHL1A\_DC10} \]
History effect: slew/load dependency

The simple inverter is analyzed.
- Variations due to HE effect are reported for both rise and fall delays.
- Variations are measured for the first transitions after a DC state 0, or 1.

Output load

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<tr>
<th>tphl_dc</th>
<th>1f</th>
<th>5f</th>
<th>10f</th>
<th>15f</th>
<th>20f</th>
<th>50f</th>
<th>100f</th>
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<tr>
<td>1p</td>
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<td>0.4</td>
<td>0.6</td>
<td>0.8</td>
<td>1.0</td>
<td>2.3</td>
<td>4.4</td>
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<tr>
<td>10p</td>
<td>0.5</td>
<td>0.5</td>
<td>0.8</td>
<td>1.0</td>
<td>1.2</td>
<td>2.5</td>
<td>4.6</td>
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<tr>
<td>50p</td>
<td>2.2</td>
<td>2.2</td>
<td>2.3</td>
<td>2.3</td>
<td>2.3</td>
<td>3.4</td>
<td>5.5</td>
</tr>
<tr>
<td>100p</td>
<td>4.4</td>
<td>4.4</td>
<td>4.5</td>
<td>4.5</td>
<td>4.5</td>
<td>4.5</td>
<td>6.6</td>
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<tr>
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<td>8.8</td>
<td>8.8</td>
<td>8.8</td>
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<tr>
<td>500p</td>
<td>21.9</td>
<td>21.9</td>
<td>21.8</td>
<td>21.8</td>
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<td>22.0</td>
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<td>43.7</td>
<td>43.6</td>
<td>43.6</td>
<td>43.6</td>
<td>44.0</td>
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<th>5f</th>
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</thead>
<tbody>
<tr>
<td>1p</td>
<td>0.2</td>
<td>0.4</td>
<td>0.6</td>
<td>0.8</td>
<td>1.0</td>
<td>2.3</td>
<td>4.4</td>
</tr>
<tr>
<td>10p</td>
<td>0.5</td>
<td>0.5</td>
<td>0.7</td>
<td>1.0</td>
<td>1.2</td>
<td>2.5</td>
<td>4.6</td>
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<tr>
<td>50p</td>
<td>2.3</td>
<td>2.3</td>
<td>2.4</td>
<td>2.4</td>
<td>2.5</td>
<td>3.3</td>
<td>5.4</td>
</tr>
<tr>
<td>100p</td>
<td>4.5</td>
<td>4.6</td>
<td>4.6</td>
<td>4.7</td>
<td>4.7</td>
<td>5.0</td>
<td>6.4</td>
</tr>
<tr>
<td>200p</td>
<td>8.9</td>
<td>9.0</td>
<td>9.1</td>
<td>9.2</td>
<td>9.2</td>
<td>9.5</td>
<td>9.9</td>
</tr>
<tr>
<td>500p</td>
<td>22.1</td>
<td>22.3</td>
<td>22.4</td>
<td>22.5</td>
<td>22.6</td>
<td>23.0</td>
<td>23.5</td>
</tr>
<tr>
<td>1000p</td>
<td>44.1</td>
<td>44.3</td>
<td>44.4</td>
<td>44.6</td>
<td>44.7</td>
<td>45.2</td>
<td>45.9</td>
</tr>
</tbody>
</table>

\[ \text{wn/wp} = 1u/2u, \ SS \ corner, -40 \, ^{\circ}C, 1.1V \]
History effect characterization

- HE is very complex and cannot be characterized exhaustively
  - Need to simplify and keep compatibility with timing analysis tools
- Use 1st/2nd switch characterization when steady-state is within reasonable range ➔ current ARM characterization
  - HE analysis is performed before characterization
  - Steady-state characterization if needed requires fast algorithm to keep control of production characterization time
- Create two SOI corners for every PVT corner
  - minsoi: minimum delay and slew
  - maxsoi: maximum delay and slew
- Ideally these corners should be mixed with local variations
- Use EDA tools capability of handling local variations
HE in design flow

- We are providing min/max SOI corners
  - instruct STA to use the min/max SOI data for -min/max OCV analysis
  - allowing for Clock Reconvergence Pessimism Removal

**SETUP**
latest arriving signal at D must arrive before the earliest arriving signal at CK

**HOLD**
earliest arriving signal at D must arrive after the latest arriving signal at CK
SOI Memory design

- SOI effects regarding the memory bitcell
  - Bipolar current during Write Operation
  - Impact of History Effect (HE) on read current
  - Dynamic read current versus DC read current

- SOI effects regarding the Sense Amplifier (S/A)
  - S/A mismatch (offset) induced by HE with FB devices
  - Use of specific SOI devices (BC MOS)
  - HE on S/A delay (w/wo Body tied devices)

- SOI effects regarding Setup, hold times, Signals races
Bipolar current & Write operation

- Assuming the column of bitcells is initialized to 1.
  - The body of pass-gates are set to a value close to 1

- When writing 0 in 1 bitcell
  - Bitline is falling
  - The body of all unselected cells is coupled low
  - But slower than the bitline

- A positive Vbe is observed

- All unselected cell have a parasitic bipolar current
  - Is it big enough to harm write functionality?
  - Has the write driver been sized accordingly
Example parasitic bipolar study

- $V_{be}=V_{bs}$ increases up to 0.32V
  - This is low enough to keep negligible the parasitic bipolar current
- This needs to be checked
  - For every technology
  - In worst case conditions
SOI effects on read current

- SRAM margin analysis (read current and signal generation)
  - Is traditionally based on a constant Iread (determined by DC simulation)
  - Plus a deviation due to local variations determined independently

- In SOI though Iread will depend on the state of the body.
  - DC analysis assumes the body has stabilized
  - Actually the transient behavior of the body changes the value of Iread
    - before WL is rising the body is lower on PG (no charge through gate & source)
    - But the body is raised when WL rises through coupling
    - It is not obvious if the body is lower or higher than in the DC case
    - Depending on the body voltage Iread may by more or less than in DC

- In addition an history effect can be observed on read current
  - Depending on activity
Transient / DC Iread: Simulation setup

- **Iread\_TRAN**
  - WL ramps from 0 to vdd
  - Iread establishes through PG & PD
  - Iread maintained through voltage source on bl

- **Iread\_DC**
  - WL is static at vdd
  - DC Iread flows through PG & PD

![Diagram](image1)

![Diagram](image2)
TRAN / DC $I_{\text{read}}$: results

- $V_{\text{body}}$ is coupled high by WL

**65nm GP cell**

<table>
<thead>
<tr>
<th></th>
<th>DC</th>
<th>TRAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{body}}$</td>
<td>0.72</td>
<td>0.65</td>
</tr>
<tr>
<td>$I_{\text{read}}$ (μA)</td>
<td>72.4</td>
<td>71.3</td>
</tr>
<tr>
<td>$\Delta I_{\text{read}}$</td>
<td>-1.5%</td>
<td></td>
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Compared to DC, TRAN $V_{\text{body}} \uparrow \Rightarrow V_{\text{TPG}} \uparrow \Rightarrow I_{\text{read}} \uparrow$

**45nm LP cell**

<table>
<thead>
<tr>
<th></th>
<th>DC</th>
<th>TRAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{\text{read}}$ (μA)</td>
<td>16.8</td>
<td>19.1</td>
</tr>
<tr>
<td>$\Delta I_{\text{read}}$</td>
<td>+13.7%</td>
<td></td>
</tr>
</tbody>
</table>

$V_{\text{body}} \uparrow \Rightarrow V_{\text{TPG}} \uparrow \Rightarrow I_{\text{read}}$

- $I_{\text{read}}_{\text{TRAN}}$ can be more or less than $I_{\text{read}}_{\text{DC}}$
  - Depending on the transistor optimization and technology node
- $I_{\text{read}}_{\text{TRAN}}$ needs to be carefully characterized
- Then only the traditional $I_{\text{read}}$ statistical margin analysis can start

Typical corner
65nm BSIMSOI3.2 SRAM spice models
Activity dependency of Read operation

- HE depends on previous state,
  - body voltages can be different
  - Thus modifying read current

- Considering 2 Read0 cycles, with DC0 & DC1 on node IT:
  - DC0-R0 (1\textsuperscript{st} switch)
  - DC1-W0-R0 (2\textsuperscript{nd} switch)

- Vbpg & Vbpd will be different
  - As a consequence Iread will be different

<table>
<thead>
<tr>
<th>IT DC0/R0</th>
<th>IT DC1/W0/R0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vbpg (V)</td>
<td>-</td>
</tr>
<tr>
<td>Vbpd (V)</td>
<td>-</td>
</tr>
<tr>
<td>Iread (\mu A)</td>
<td>41</td>
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</table>
Conclusion on Iread

- Traditional (bulk) DC Iread simulation is not accurate for SOI

- Transient behavior must be analyzed for each technology
  - Behavior may vary for different transistors \((\text{tran} > \text{dc}, \text{dc} > \text{tran})\)
  - Trends may vary depending on the transistor parameters \((\text{coupling, leakage…})\)
  - Initial DC State needs to be carefully select for simulations

- Needs some engineering work
  - Methodology and simulation update for each technology
- For repeated read cycle in the same state, a body voltage differential develops between BNB & BNT, BPB & BPT.
  - Example above: read 0, implies VBNB rising while VBNB decreasing.
  - The body voltage difference can be reduced with body contacted transistors.
Sense Amp alternative body connections

- Fully floating body (SA3) is not selected for SOI technology
  - The speed gain is wasted into extra margin required for functionality
- Body contacted transistors are used
  - Still at high frequency, and repeated 'read1' or 'read0' a difference between the two matched transistors can develop.
  - The subsequent systematic offset needs to be limited by design
Body tied to ground transistor simulation

- A careful analysis of history effect on BT transistors
  - Is required on a technology by technology basis
- To determine the best compromise for transistor Width
  - Minimize history effect across body
  - Minimize mismatch (maximizing gate area)
History effect in SRAM self timed loops

- Proper design style leads to drastic reduction of history effect (50ps → 1ps)

A 500ps input slope is applied on CK pin
WC corner for History effect (SS, -40°C, 1.1V)
Conclusion

- A variety of SOI effects must be studied and quantified
  - AC behavior, History effect & DC state, parasitic bipolar, body behavior…
  - Can not be neglected to check functionality
  - Are to large to simply include in margin

- SOI dedicated engineering is key
  - Magnitude of effects are technology dependent
  - SOI effects can be limited by good design practice
    - SOI benefits can be lost by design (e.g simple SOI/Bulk porting)

- ARM has the SOI IP design know-how and flows in place
  - Physical IP design style adapted for each project
    - Experienced SOI designers
  - IP development infrastructure is adapted for SOI
  - SOI challenges are transparent to the IP end users
    - standard EDA flow can be used
    - IP logic functionality and interface identical to bulk