Design of NaviEngine
- a SoC with MPCore -

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Agenda

- Background
  - Automotive Multimedia Markets
  - Multicore Technology
- Concept of NaviEngine®
- System solution
  - Hardware Platform
  - Software and tools
- Future roadmap
Future Car system

More Comfort • Safety • Environment
- easy and fun to drive
- safety and relax
- Earth friendly

- Entertainment (Video and Audio)
- ITS (VICS/DSRC/WAN/LAM)
- Easy user Interface
- Security

- Driver assist
  - Camera and recognition
- Pre clash safety
  - air bag control
  - emergency alert

- Fuel cell car
- Hybrid car
- Traffic jam free

Evolution in Car for better Society
Evolution of Car Infotainment Systems

Navigation ⇒ Entertainment ⇒ Driver assistance ⇒ Intelligent Car

Brain of Car, face to driver and passenger.

Multiple application combined in single unit.

- TV Phone
- Camera
- Browser
- Voice
- Mail
- Digital Navigation
- Image recognition
- 3D Graphics
- Speech Recognition
- JAVA
- Security

Future = 20,000MIPS

ECU integration
- Body ECU, Engine ECU

Intelligent car
- Auto Drive

Next Gen = 2,000MIPS

Now = 600MIPS

2005
2010
2015

Now=600MIPS
Multiple application combined in single unit.

TV Phone
Camera
Browser
Voice
Mail
Digital Navigation
Image recognition
3D Graphics
Speech Recognition
JAVA
Security

Future = 20,000MIPS

Intelligent car
- Auto Drive

Next Gen = 2,000MIPS

Now=600MIPS
Requirement for CPU

① Low Power for In dashboard ⇒ Embedded product
power range

② High performance ⇒ Over 1000MIPS

③ Easy to use ⇒ Real-time response for UI

④ Many Products for Many country ⇒ Minimize design cost and resource

PC & Server
Embedded
Mobile

0.1W 1W 10W 100W

UI 80MIPS
Traffic info 100MIPS
Digital TV 200MIPS
Vision recog 400MIPS
Navigation 400MIPS

Beep! Car approaching

Hey, where it is?

Car Maker A
Asia
US
Europe

Car Maker B
Asia
Europe
US
Merit of Multicore: High performance and low power

Parallel processing technology

Relationship between processing speed and power consumption

- Increase frequency → Larger power consumption
- Parallel processing → Improved power consumption

Diagram showing:
- Power Consumption
  - High
  - Medium
  - Low
- Performance (MIPS)
  - 500
  - 1000
  - 1500
  - 2000
  - 2500
- Speed up
- Single high frequency CPU
- Parallel processing
- 1CPU core
- 2CPU core
- 3CPU core Multi Processor

(NEC Electronics estimate)
## Merit of Multicore: Real Time Response

The real-time response is improved by dispatch tasks to individual CPUs.

<table>
<thead>
<tr>
<th>Single CPU</th>
<th>Total Task time</th>
<th>Real-time</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td><img src="image" alt="Diagram" /></td>
<td>Time slice of scheduling tasks is bottle neck of response.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multi CPU</th>
<th>Total Task time</th>
<th>Real-time</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU1</td>
<td><img src="image" alt="Diagram" /></td>
<td>If there are free CPU, task can be dispatched with minimum overhead.</td>
</tr>
<tr>
<td>CPU2</td>
<td><img src="image" alt="Diagram" /></td>
<td>Or, dispatch task statically with specific CPU to zero overhead.</td>
</tr>
<tr>
<td>CPU3</td>
<td><img src="image" alt="Diagram" /></td>
<td></td>
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</tbody>
</table>
Scalable Platforms

Scalable architecture built on parallel processing technology and media processing technology

Best balance for Power, performance and cost

High

Application SW for single CPU designs can also be used for multiple CPU designs

Low

Simple functions

Complex functions

Select number of CPUs based on balance between need for power consumption and performance

Sharing of functions and loads

NEC ELECTRONICS
NEC’s Multicore Technology

NEC has over 10 year history and expertise in Multicore technology R&D for embedded market.

MP98 Technology:
1. High performance on-chip multicore design
2. Low power consumption with adaptive shutdown
3. Software technology to hide complexity of multicore.

MP211 (Jan. 2005)

2000, MP98 announcement

Parallel S/W (Sept. 2004)

SMP technology

MPcore

NaviEngine1

MPCore
IOs
2D/3D
LCDC

Media Parallel “IMAP”

8SIMD Core
16 Cores on Chip = 128 Processor
Strategic Collaboration

In 2003, ARM and NEC Electronics established a strategic collaboration for next generation CPU core development.

ARM
- ARM11™ core
- Widely-deployed ARM family with rich line-up of software and development environments

NEC Electronics
- Multiprocessing technology
- High performance and low power LSI design technology

◆ Collaboration
1. Next generation parallel CPU core co-development and co-marketing
2. Fundamental software development

1st result: MPCore™
Concept of NaviEngine

Product definition:

- 1st product to use NaviEngine Architecture
  - ARM SMP: Multicore for scalability
  - AXI and MBus: High performance bus interconnect
  - SGX: Embedded 2D/3D Graphics capability
  - On-chip multiple IOs (LCDC, SATA, etc.)

- Establish NaviEngine platform
  - Multicore ICE and OS will be prepared
  - Software (Middleware and application) development bench
### NaviEngine Specification overview

- **power supply (VDD)**: 1.0V, 1.8V, 3.3V
- **power consumption (PD)**: 5W (T.B.D.)
- **storage temperature (TST)**: 65~125°C
- **operative temperature (Tc)**: 40~105°C

*(※)The measurement point of Tc is the center of lid.*

<table>
<thead>
<tr>
<th>Function</th>
<th>contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td><strong>MPCore (ARM11 × 4)</strong> 400MHz, with VFP11</td>
</tr>
<tr>
<td>i-cache/d-cache</td>
<td>32kbyte/32kbyte</td>
</tr>
<tr>
<td>Local Memory</td>
<td>1kbyte</td>
</tr>
<tr>
<td>Others</td>
<td>MMU, JAVA accelerator</td>
</tr>
<tr>
<td>Memory controller</td>
<td><strong>DDR2 (533 × 32bit)</strong></td>
</tr>
<tr>
<td>Graphics</td>
<td><strong>SGX535</strong> (8Mline/s, 15Mpoly/s, 800M pix/sec)</td>
</tr>
<tr>
<td>Peripherals</td>
<td><strong>Display Controller</strong> W-SVGA 7 layer (max)</td>
</tr>
<tr>
<td></td>
<td><strong>Video Capture</strong> ITU-R BT.601/ITU-R BT.656 RGB565/RGB888</td>
</tr>
<tr>
<td></td>
<td><strong>Others</strong> USBH2.0, SATA/ATA, UART, CSI, SPDIF, I2S, etc.</td>
</tr>
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720pin (0.8mm) FCBGA
Software development platform

- General purpose software development platform for NaviEngine
- Not for Hardware evaluation
  - Design for typical use-case only
- Low cost, easy to use
  - Small foot print for desk top work
- Compliant for T-Engine design
  - Plug in board and peripherals will be available.
**Three bottlenecks in multiprocessing**

- Sequential Part
- Load imbalance
- Communication overhead

**Example:** System activity consists of 4 tasks (or 4 threads)
Performance Analysis and Tuning

Run existing application set on SMP OS.

(If the sequential part is small or load is well balanced we will get enough performance.)

- Relax the synchronization point of sequential part by modifying algorithm, etc.
- Tune the communication code.

- Find the key components (e.g. 1) and restructure it with multithreading.

Profiling tool is useful for the tuning.
Summary

- Car Navigation will evolve to Brain in the car with CPU performance improvement.
- Multicore is Key factor to realize such high performance as in-car system
- Prepare to support Multicore will take advantage for coming business in embedded electronics
- NEC will provide semiconductor platform to open the door for this.

Thank you!
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